

Notice of References Cited	Application/Control No. 10/814,106	Applicant(s)/Patent Under Reexamination JOLLY ET AL.	
	Examiner Matthew D. Spittle	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Savoj, Jafar. A 10-GB/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector. IEEE Journal of Solid-State Circuits. Vol. 36, No. 5, May 2001.
	V	Arimoto et al. A Speed-Enhanced DRAM Array Architecture with Embedded ECC. IEEE Journal of Solid-State Circuits. Vol. 25, No. 1, February 1990.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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